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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/713,971	IEONG ET AL.
	Examiner	Art Unit
	Stanetta D. Isaac	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-14 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-14 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 5/11/05. Currently, claims 10-14, 16-20 and newly added 21 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-12, 14 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soutome US Patent 6,010,921 in view of Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Second Edition, Lattice Press, 2000, pages 202, 421-423 and 833-834.

Soutome discloses the semiconductor method substantially as claimed. See figures 1A-7D, and corresponding text, where Soutome shows pertaining to claim 10, a method of fabricating a recessed channel CMOS device comprising the steps of: providing a patterned oxide layer **5** over an SOI layer **3**, said patterned oxide layer exposing a portion of said SOI layer (figure 3B; col. 7, lines 12-17); thinning the exposed portion of the SOI layer to form a recessed channel region (figures 3A-3B; col. 7, lines 13-33); forming a gate dielectric **9** on said recessed channel region (figure 3D; col. 7, lines 59-60); forming sacrificial spacers **8** on portions of said gate dielectric so as to protect exposed walls of said SOI layer and said oxide layer (figure 3C; col. 7, lines 41-48) and forming a gate conductor **10** on the other portions of the gate dielectric

not containing said sacrificial spacers (figure 3D; col. 7, lines 59-67; col. 8, lines 1-2); recessing the oxide layer exposing SOI layer abutting the recessed channel region (figure 3E; col. 8, lines 3-6); forming a source/drain diffusion regions **19** in said exposed SOI layer abutting the recessed channel region (figure 3E; col. 8, lines 7-14); and removing the sacrificial spacers and forming extension implant regions **18** in said SOI layer such that said extension implant regions have an abrupt lateral profile and are located beneath the gate conductor (figure 3E-3F; col. 8, lines 42-67; col. 9, lines 1-6, broadly interpreted, the extension regions are in a lower position than that gate conductor). In addition, Soutome shows, pertaining to claim 11, the method, wherein said thinning is carried out by chemical downstream etching, reactive-ion etching, or thermal oxidation and etching (figures 3A-3B; col. 7, lines 13-33, thermal oxidation and etching). Also, Soutome shows, pertaining to claim 12, the method wherein said thinning is carried out by thermal oxidation and a chemical oxide removal process (figure 3E; col. 8, lines 3-6). Soutome shows, pertaining to claim 14, the method, wherein said source/drain diffusion regions are formed by ion implantation and annealing (figures 3E-3F; col. 8, lines 42-67; col. 9, lines 1-6). In addition, Soutome shows, pertaining to claim 16, the method, wherein further comprising forming permanent spacers **13** on exposed sidewalls of said gate conductor and said gate dielectric (figure 3F; col. 8, lines 19-26). Also, Soutome shows, pertaining to claim 17, the method wherein said gate conductor is a polysilicon gate conductor that is formed by deposition and ion implantation (col. 8, lines 7-12). Finally, Soutome shows, pertaining to claim 18, the method further comprising forming trench isolation regions **4** in said SOI layer (col. 7, lines 13-15)

However, Soutome fails to show, pertaining to claim 10, the method comprising forming sacrificial nitride spacers on portion of said gate dielectric so as to protect exposed walls of said SOI layer and said oxide layer and forming a gate conductor on the other portions of the gate dielectric not containing said sacrificial nitride spacers; and removing the sacrificial nitride spacers and forming extension implant regions in said SOI layer such that said extension implant regions have an abrupt lateral profile and are located beneath the gate conductor. In addition, Soutome fails to show, pertaining to claim 19, the method further comprising forming halo implant regions after forming said extension implant regions, said halo implant regions having a abrupt lateral profile which are located beneath said gate conductor. Also, Soutome fails to show, pertaining to claim 20, the method wherein said halo implant regions are formed by angled implantation and annealing. Finally, Soutome fails to show, pertaining to claim 21, the method, further comprising forming extensions implant regions angled implantation and annealing.

Wolf teaches, pages 202, 421-423 and 833-834, the conventionally known properties of silicon nitride material. In addition, Wolf teaches, conventional shallow junction formation techniques that include the halo implantation for CMOS devices. Also, Wolf teaches, conventional angled implant techniques used in shallow junction formations specifically for halo implantation.

It would have been obvious to one of ordinary skill in the art to substitute, the method comprising forming sacrificial nitride spacers on portion of said gate dielectric so as to protect exposed walls of said SOI layer and said oxide layer and forming a gate conductor on the other portions of the gate dielectric not containing said sacrificial nitride spacers; and removing the sacrificial nitride spacers and forming extension implant regions in said SOI layer such that said

extension implant regions have an abrupt lateral profile and are located beneath the gate conductor, in the method of Soutome, pertaining to claim 10, according to the teachings of Wolf, with the motivation that, the silicon nitride, taught by Wolf, is conventionally used as sidewall spacers for MOSFET devices, for the purpose of creating lightly-doped drain (LDD) structures. In addition, conventionally the properties of silicon nitride are advantageously suitable for passivation layers, based on its ability to protect against diffusion of impurities, subjection to severe environmental stress, and its deposition of acceptably low pinhole density.

It would have been obvious to one of ordinary skill in the art incorporate, the method, further comprising forming halo implant regions after forming said extension implant regions, said halo implant regions having a abrupt lateral profile which are located beneath said gate conductor; the method wherein said halo implant regions are formed by angled implantation and annealing; the method, further comprising forming extensions implant regions angled implantation and annealing, in the method of Soutome, pertaining to claims 19, 20 and 21, according to the teachings of Wolf, with the motivation that, the source/drain extension implant regions, taught by Wolf, are conventionally formed within CMOS devices, where an improvement to the CMOS device would be to perform a halo implantation of 0° or a high 30° tilt angle, for the purpose of increasing abruptness to the extension junction doping profile, decreasing the extension junction depth, and increasing the punch-through voltage.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soutome US Patent 6,010,921 in view of Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Second Edition, Lattice Press, 2000, pages 202, 421-423 and 833-834, in further view of Torek et al., US Patent 5,685,951.

Soutome in view of Wolf discloses the semiconductor substantially as claimed. See the preceding rejection of claims 10-12 and 14-20 under 35 U.S.C. 103(a).

Soutome in view of Wolf fails to show, pertaining to claim 13, the method, wherein said COR process is carried out at relatively low pressure of 6 millitorr or less and in a vapor of HF and NH_3.

Torek teaches, in figures 1-3, and corresponding text, the advantages of etching a thermal oxide material with a vapor phase system, that includes the use of a vapor of hydrofluoric (HF) and ammonia (NH_3) (col. 5, lines 30-48; col. 7, lines 15-20).

It would have been obvious to one of ordinary skill in the art to, substitute, the method, wherein said COR process is carried out at relatively low pressure of 6 millitorr or less and in a vapor of HF and NH_3, in the method of Soutome in view of Wolf, pertaining to claim 13, according to the teachings of Torek, with the motivation that, the vapor phase etching, taught by Torek, results in an increased removal of thermal oxide. In addition, the vapor phase etching method, taught by Torek, requires a decreased amount of chemical usage, that reduces etching procedures, resulting in a more environmentally safe and economically beneficial etching process. Finally, based on the teachings of Soutome in view of Wolf in further view of Torek, a relatively low pressure of 6 millitorr or less would be considered within routine experimentation, since conventionally used processing techniques are performed in the formation of the semiconductor devices.

Response to Arguments

Applicant's arguments filed 5/11/05 have been fully considered but they are not persuasive.

In response to the Remarks, pages 4-9:

The Applicant raises the clear issue, whether Soutome taken alone or in combination of Soutome in view of Wolf in further view of Torek, suggests sacrificial nitride spacers on a portion of the gate dielectric, suggests the presence of sacrificial spacers during the fabrication of the recessed channel and the source/drain regions, or suggests modifying in such a way to remove sacrificial spacers after formation of the source/drain regions and just prior to formation of the extension implant regions.

The Examiner takes the position that a method of fabricating a recessed channel CMOS device as shown by the combined teachings of Soutome in view of Wolf in further view of Torek would lead one of ordinary skill in the art to substitute the sacrificial oxide spacers with a sacrificial nitride spacer for the purpose of creating more efficient sidewall spacers used to protect the exposed walls of the SOI layer, as taught specifically by Wolf. With regards to the removal of the "sacrificial spacers after formation of the source/drain regions and just prior to formation of the extension implant regions." This limitation is not claimed and, as a result, arguments are rendered moot. The claims only calls for "removing the sacrificial nitride spacers and forming extension implant regions in said SOI layer such that said extension implant regions have an abrupt lateral profile and are located beneath the gate conductor." Regarding the sacrificial nitride spacers, in figure 3C and as stated in col. 7, lines 41-48, Soutome teaches, the

formation of sacrificial spacers (oxide material) on portions of the gate dielectric so as to protect the exposed walls of the SOI layer. It takes the added teaching of Wolf to realize the benefits of using a silicon nitride material as a spacer, where the conventional properties of silicon nitride are advantageously suitable for passivation layers, based on its ability to protect against diffusion of impurities, subjection to severe environmental stress, and its deposition of acceptably low pinhole density, resulting in a more reliable protection layer. Therefore, it would be more desirable to substitute the sacrificial oxide spacers with sacrificial nitride spacers based on the above advantages to create a more efficient protection layer for the exposed walls of the SOI layer.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
July 19, 2005

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